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(54) **Semiconductor device provided with a programmable element**

Halbleitervorrichtung mit einem programmierbaren Element

Dispositif semi-conducteur comportant un élément programmable

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- **PATENT ABSTRACTS OF JAPAN vol. 9, no. 212 (E-339)(1935) 29 August 1985 & JP-A-60 074 669 (FUJITSU LTD.) 26 April 1985**

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Description

[0001] The invention relates to a semiconductor device with a programmable element comprising a doped semiconductor region and a conductor region which are separated from one another by at least a portion of an insulating layer, said insulating layer having a thickness such that, during programming, breakdown may occur in the insulating layer upon applying a voltage between the conductor region and the semiconductor region, the conductor region comprising a material which is suitable for forming a rectifying junction with the material of the semiconductor region, while the programmable element is provided with a contact region which forms an ohmic contact with the semiconductor region and which has a comparatively low electrical resistivity compared therewith.

[0002] The invention in particular relates to a semiconductor device in which such a programmable element forms part of an electrically programmable memory cell which is arranged in a matrix of a number of similar memory cells.

[0003] Such a semiconductor device is known from US Patent 4,881,114, where the programmable element is used in a programmable memory cell. The known programmable element comprises a semiconductor region in the form of a boron-doped p-type surface zone which is situated in an n-type substrate of monocrystalline silicon. The conductor region of the known element is formed by a portion of a comparatively heavily n-type doped polycrystalline silicon layer which is separated from the p-type surface zone by a triple insulating layer of silicon oxide; silicon nitride and silicon oxide in that order.

[0004] The element can be programmed in that a voltage difference is applied between the semiconductor region and the conductor region to such a value that the insulating layer breaks down at least locally. Where the insulating layer shows breakdown, the p-type silicon of the semiconductor region and the n-type silicon of the conductor region come into mutual contact, thus forming a rectifying pn junction. In this state, the element has a comparatively low resistance at least in the forward direction of the pn junction, in contrast to the unprogrammed state in which the element is non-conducting.

[0005] For the purpose of electrically connecting the semiconductor region, the programmable element is provided with a contact region which has a substantially lower electrical resistance than the semiconductor region itself. The contact region in the known device comprises a surface zone which is comparatively heavily p^+-type doped and which adjoins the semiconductor region.

[0006] The contact region does provide a comparatively good conductive connection to the memory element, but it requires additional surface area in the known device, which is to the detriment of the packing density and renders the known memory cell in particular less suitable for large-scale integration.

[0007] In US-A 5,126,290 a programmable structure is described with polysilicon digit lines, the sidewalls of which are covered with a dielectric forming the antifuses and with polysilicon forming overlying word lines. In this known device, the digit lines are not provided with a low-ohmic contact region.

[0008] In US-A 3,774,170 a memory is disclosed utilizing Schottky diodes which are guided for one column over a buried layer provided at the interface between a silicon substrate and an epitareial layer. This known device is mask-programmed and can not be programmed by the user. Moreover, for the island isolation in the column direction, in the n-type epitareial layer, deep p-type zones are used, forming a reversely biased pn-junction with the epitareial layer.

[0009] From JP-A 60-74669 a mask-programmed ROM and BIC memory is known in which the diodes are laterally bounded by a dielectric isolation region.

[0010] In EP-A-0 216 246 a BIC memory is described in which the programmable elements contact a buried bit line.

[0011] The invention has for its object to provide a semiconductor device of the kind mentioned in the opening paragraph for which only a relatively small surface area at the semiconductor surface is required.

[0012] According to the invention, a semiconductor device of the kind mentioned in the opening paragraph is characterized in that the contact region is provided at a side of the semiconductor region remote from the insulating layer and is separated from the insulating layer by the semiconductor region, and in that both the semiconductor region and the contact region are laterally bounded by a dielectric insulation region at mutually opposing sides.

[0013] In the device according to the invention, accordingly, the contact region is vertically integrated with the semiconductor region. As a result, it does not occupy any space in lateral direction, so that no additional chip surface area is required for the contact region. The space required for the programmable element may thus be limited to the surface area of the semiconductor region alone, and thus to the minimum lithographic dimension, *i.e.* the dimensions of the smallest detail which can still be adequately pictured without problems, given a certain lithography. For a minimum lithographic dimension ℓ, according to the invention, no more than C space is required for the programmable element.

[0014] A special embodiment of the device according to the invention is characterized in that both the semiconductor region and the contact region form part of a first strip-shaped conductor track which is laterally bounded by the insulation region and in that the conductor region forms part of a second strip-shaped conductor track which extends transverse to the direction of the first conductor track. The programmable element in this embodiment is situated at the overlap of the two con-

ductor tracks. The surface area required for this is equal to the product of the widths of the two conductor tracks. Both widths can be reduced to the minimum lithographic dimension ℓ, so that the programmable element itself requires no more than ℓ^2 space. The conductor tracks may serve, for example, as selection lines, *i.e.* as word and bit lines by means of which the programmable element may be addressed so as to be read or programmed.

[0015] It is noted in this connection that, wherever a conductor is referred to in the present application, within the scope of the invention this should be understood to mean any material capable of conducting an electric current. This definition in particular comprises not only metals, metal alloys and metal compounds, but also semiconductor materials.

[0016] The insulation region which bounds the semiconductor region may comprise, for example, an oxide region which was obtained through local oxidation of semiconductor material. A preferred embodiment of the invention, however, is characterized in that the insulation region comprises a groove which bounds the semiconductor region laterally and which is coated with at least an insulating layer. In particular when the semiconductor body comprises a number of similar programmable elements, a much higher packing density can be realised by means of groove insulation than by means of a insulation region obtained through local oxidation. The mutual interspacing between elements is in fact determined not only by the lithographic and technological accuracy, but also, and indeed in the case of high packing densities even mainly by the minimum length of the current path between adjoining elements which is necessary for avoiding breakdown effects, especially latch-up, between adjoining elements. This length is often greater than the minimum lithographic dimension especially in modern semiconductor processes. When groove insulation is used according to the invention, it is achieved that the current path between adjoining elements extends for a comparatively major part in the depth direction without requiring additional space for this purpose in lateral direction. The lateral distance between adjoining elements can thus remain limited to the minimum lithographic dimension, so that a very high packing density can be realised. The width-depth ratio of an insulation region formed by local oxidation is in general too great for achieving the same packing density.

[0017] The desired groove insulation may be formed, for example, through local removal of material from an otherwise continuous semiconductor layer, for example through etching, in which case the layer itself may be used for forming the semiconductor region. The insulation region and the semiconductor region are thus automatically aligned relative to one another, so that a mutual alignment step is avoided. In addition, removal techniques with an anisotropic action known *per se* may be used for etching of the groove, so that a lateral extension of the insulation region can be restricted to a minimum. The lateral dimension of the insulation region in that case is substantially entirely determined by the lithography used and may thus be reduced to the minimum lithographical dimension ℓ. In this preferred embodiment, the memory cell according to the invention including the accompanying insulation region does not require more than $4\ell^2$ surface area. This is considerably less than the surface area needed for the known programmable element.

[0018] Furthermore, this preferred embodiment leads to a comparatively simple structure, at least as far as the programmable element is concerned. As a result, the device is particularly suitable for use of so-called phase shifting techniques which are known *per se* in present-day lithography and by which details can be pictured of approximately half the size of what would otherwise be possible. The use of such a technique renders it possible to reduce the surface area required for a programmable memory cell including the accompanying insulation region to ℓ^2, which is an order of magnitude smaller than the total surface area required for the known memory cell including its insulation region.

[0019] This means, for example, that in modern optical lithography with a minimum lithographic dimension ℓ of 0.5 μm with the use of phase shifting techniques a memory cell can be realised on a surface area of no more than 0.25 μm^2 in the device according to the invention. Thus some 400 million memory cells per cm^2 chip surface can be integrated in the device according to the invention. This corresponds to an information density of 400 Mbit/cm^2, which is an order of magnitude higher than what can be achieved in known memories using the same lithography. The invention is accordingly extremely suitable for applications in which a very large memory capacity is required such as, for example, as an audio and/or video memory or as a memory in computer equipment.

[0020] Smaller details can be pictured and the integration may be increased even further in that illumination is carried out not with visible light but with radiation of a shorter wavelength such as, for example, UV radiation and X-ray radiation, or electron radiation.

[0021] The construction of the programmable element according to the invention is comparatively simple, and accordingly comparatively simple process steps are required for its manufacture, which steps may in addition be carried out in a comparatively late stage of a conventional semiconductor manufacturing process. This renders it possible in particular to provide the element only after a semiconductor switching element has been formed in a semiconductor body, and to place the programmable element on the switching element, separated therefrom by a dielectric intermediate layer. In this manner, for example, any control electronics of the element can be integrated below the cell, so that no additional chip surface area is required for that purpose.

[0022] The invention will now be explained in more

detail with reference to a few embodiments and a drawing, in which:

Fig. 1A is a cross-section of a first embodiment of the semiconductor device according to the invention comprising a programmable memory cell;

Fig. 1B shows the device of Fig. 1A with a memory cell after programming;

Fig. 2A is a perspective view of a second embodiment of the semiconductor device according to the invention;

Fig. 2B is a plan view of the device of Fig. 2A; and

Fig. 3 is a cross-section of a third embodiment of the device according to the invention.

[0023] The Figures are purely diagrammatic and not drawn to scale. Some dimensions in particular are shown strongly enlarged for the sake of clarity. Semiconductor regions of the same conductivity type are hatched in the same direction as much as possible, and corresponding parts are given the same reference numerals.

[0024] In a first embodiment, the programmable element according to the invention is used in a memory cell which is integrated into a silicon semiconductor body with an n-type surface region 1, sec Fig. 1A. The element comprises a semiconductor region in the form of a boron-doped p-type semiconductor zone 4 which is situated in the surface region 1 and adjoins the surface 2 of the semiconductor body. The p-type surface zone 4 is separated from a conductor region 6 by an approximately 8 nm thick insulating layer 5 of silicon oxide. The conductor region 6 in this embodiment comprises n-type silicon and forms part of a comparatively heavily doped polycrystalline layer 16. Instead of silicon of a doping type opposite to that of the surface zone 4, a Schottky metal which is suitable for forming a rectifying Schottky junction with the silicon of the surface zone 4, may alternatively be used for the layer 16 and the conductor region 6, if so desired. The comparatively low resistivity of the layer 16 in that case ensures a comparatively low-ohmic connection to the conductor region 6.

[0025] The memory cell is further provided with a contact region which, according to the invention, is applied to the side of the p-type surface zone 4 remote from the insulating layer 5. The contact region is formed by a comparatively heavily p-type doped buried zone 3. Both the surface zone 4 and the buried zone 3 are bounded by an insulating region 7 at opposing sides according to the invention. The insulating region 7 comprises a silicon oxide region which is partly recessed into the semiconductor body 1 and which was obtained through local oxidation (LOCOS) of the semiconductor body.

[0026] The contact region 3 is provided below the surface zone 4 through an implantation with ions comprising boron after the formation of the insulating region 7. A comparatively large dose and a comparatively high implantation energy of 10^{15} ions/cm^2 and 200 keV, respectively, were used during this treatment. The insulating region 7, however, is sufficiently thick for forming an effective mask against the implantation of the contact region 3. The contact region 3 is thus formed automatically in the correct spot.

[0027] Because of the comparatively heavy dose, the contact region 3 has a comparatively high doping concentration and thus a comparatively low sheet resistance compared with the surface zone 4. The contact region 3 accordingly provides a sufficiently low-ohmic connection to the semiconductor region 4.

[0028] Thanks to the invention, the memory cell within the oxide region 7 does not require more space than does the surface zone 4 on its own. The width thereof was taken as small as possible in the present example, for a given lithography, so that it is equal to the minimum lithographic dimension ℓ of 0.5 µm. The same holds for the width of the conductor region 6. The present memory cell itself accordingly does not occupy more than 0.25 µm^2 chip surface area. This is considerably less than what is required for a conventional memory cell, given the same lithography.

[0029] The memory element is programmed in that a short pulse is applied between the p-type surface zone 4 and the silicon layer 6 of a sufficiently high voltage for causing an electric breakdown at least locally in the interposed silicon oxide layer 5. Fig. 1B shows the memory cell in the programmed state. The n-type silicon of the conductor region 6 and the p-type silicon of the semiconductor region 4 come into mutual contact where the oxide layer 5 was punctured, and a rectifying pn junction 8 is formed. It should be noted in this connection that, although the rectifying junction 8 is drawn exclusively in the surface zone 4, it is possible in practice for material of the semiconductor region 4 to penetrate through the opening in the insulating layer 5 into the conductor layer 6. In that case the rectifying junction 46 will lie at least also in the conductor region 6 after programming.

[0030] A negative programming voltage is preferably applied to the silicon layer 6 relative to the p-type surface zone 4 during programming. In that case, an accumulation layer is induced into the surface zone 4 at the surface, *i.e.* a layer having an increased density of free charge carriers, whereby the programming voltage will be present entirely across the oxide layer 5. This means that a lower programming voltage can suffice compared with the situation in which an opposite polarity were applied, whereby free charge carriers would indeed be driven away from the surface and the programming voltage would partly occur across the depletion region generated thereby. In the present example, a programming voltage of -12 V is found to be sufficient already for programming the cell. If the semiconductor region 4 were oppositely doped, *i.e.* n-type, the same would apply *mutatis mutandis*. In that case, the polarity of the programming voltage is adapted accordingly and

a positive voltage difference of the conductor region 6 relative to the semiconductor region 4 is preferably applied. The doping concentration in the polycrystalline silicon layer 16, 6 is so high that no depletion region of any importance is created therein.

[0031] Included in a matrix, the memory cell may be selected for programming in that the silicon layer 16 is used as a first selection line and a programming voltage of -12 V is applied thereto relative to the contact region 3 which may be used as a second selection line, and in that an opposite voltage difference is applied between each corresponding first and second selection line of the remaining selection lines of the matrix. In that case, exclusively the desired cell is programmed because only in that cell 12 V will actually be across the insulating layer 5. In non-selected non-programmed cells, across which the programming voltage will be applied with opposite polarity, indeed, a portion of the programming voltage will be present across the depletion region induced into the surface zone 4 in that case.

[0032] It is possible in this method of addressing for the offered programming voltage to fall across the pn junction 8 formed therein as a reverse bias voltage in a cell which has been programmed. This means that the breakdown voltage of the pn junction 8 must be greater than the programming voltage used. Since the series resistance of the cell is mainly determined by the comparatively well-conducting contact region 3 and the also comparatively well-conducting silicon layer 16, and is influenced only to a slight degree by the specific doping concentration of the comparatively short semiconductor region 4, the doping concentration of the semiconductor region 4 may be freely adapted so as to comply with this requirement without the total series resistance of the element being excessively increased. In the present example, a boron concentration of approximately 10^{16} cm^{-3} is used for the surface zone 4, so that the breakdown voltage of the junction 8 formed is amply sufficient for withstanding the programming voltage of 12 V.

[0033] A second embodiment of the device according to the invention is shown in perspective view in Fig. 2A. Fig. 2B is a plan view of the same device. A number of insulating layers which usually cover and passivate the device have been left out in both Figures for the sake of clarity.

[0034] In this embodiment, the device comprises a matrix of memory cells, which matrix is formed by a number (n) of parallel first strip-shaped conductor tracks 24 which extend in a first direction and of which four have been depicted, and by a number (m) of parallel second strip-shaped conductor tracks 26 which extend in a second direction transverse to the direction of the first conductor tracks and of which three are shown in the Figure. Both the first and the second conductor tracks in this embodiment are formed by semiconductor tracks of silicon. The first conductor tracks 24 are of monocrystalline structure and are p-type doped with boron. The second conductor tracks 26 on the other hand comprise polycrystalline silicon and are oppositely, *i.e.* n-type, doped with arsenic. The two kinds of conductor tracks 24, 26 are separated from one another by an insulating layer 5 in the form of an approximately 10 nm thick so-called ONO layer of, in that order, approximately 2 nm silicon oxide, approximately 6 nm silicon nitride, and approximately 2 nm silicon oxide.

[0035] The p-type first conductor tracks 24 are provided on an n-type type silicon substrate 1 and each form a pn junction 21 therewith. The pn junctions are reverse biased during operation and ensure an adequate electrical isolation of the conductor tracks 24 relative to the substrate 1 and relative to one another.

[0036] The first conductor tracks 24 are laterally bounded by strip-shaped insulating regions 27 in the form of longitudinal grooves whose walls are coated with an insulating layer 28 of silicon oxide. The grooves 27 are filled up further with a suitable filler 29 in a manner known *per se*. In this embodiment the grooves 27 are filled with polycrystalline silicon, which is subsequently covered with silicon oxide by means of a short oxidation step.

[0037] The memory elements of the memory cells are present at the areas where a second conductor track 26 crosses a first conductor track 24. The second conductor tracks 26 constitute n-type silicon conductor regions 6 of the memory elements, and the first conductor tracks 24 constitute associated semiconductor regions 4 of p-type silicon. Below the semiconductor regions 4 there are comparatively heavily doped contact regions 3 in the form of p-type buried layers which ensure a sufficiently low-ohmic connection to the respective semiconductor regions 4.

[0038] The first conductor tracks 24 are manufactured from a p-type silicon layer which was grown epitaxially on the n-type substrate 1. The doping required for the layer is added during or after growth. Previously, the n-type substrate 1 was heavily p-type doped at its surface in order that a comparatively heavily doped p-type buried layer is created at the interface between the substrate and the epitaxial layer, which buried layer forms the contact regions 3.

[0039] After the epitaxial growth, the formed silicon layer is provided with the grooves 27 at the surface 2 by locally etching the layer using a suitable mask. The grooves 27 are etched up to and into the substrate 1 so as to ensure a good lateral isolation of adjoining conductor tracks 24. No alignment step with the accompanying alignment tolerances is required in this manner between the first conductor tracks 24 on the one hand and the insulating region 27 on the other hand, which saves space. The grooves are covered in a manner known *per se* with the dielectric layer 28 and filled with polycrystalline silicon 29. The groove may be opened at the bottom before filling. In that case the filler is connected to the substrate in the final device, so that it is prevented that the filler could act as a floating capacitor plate during operation and thus adversely affect the

operation of the device.

[0040] Anisotropic etching of the grooves 27 reduces the lateral dimension thereof to a minimum, so that also the smallest possible chip surface area is lost thereby. For this purpose, for example, an anisotropically operating plasma which is known *per se* is used as the etchant. The width of both the first conductor tracks 24 and the grooves 27 is thus determined substantially only by the etching mask used, and thus depends only on the accuracy of the lithography used. In the present example, a lithography with a minimum lithographical dimension of 0.5 µm and including phase-shifting techniques is used, and the width of the grooves and the conductor tracks is no more than approximately 0.25 µm. The depth of the grooves, however, is more than 1 µm, so that the length of the current path between adjoining cells is sufficiently great for avoiding breakdown between adjoining cells in spite of the small groove width.

[0041] The second conductor tracks 26 are manufactured in an analogous manner from a continuous n-type polycrystalline silicon layer which is provided over the entire surface and is subsequently etched into a pattern with an anisotropic etchant. As a result, again, the second conductor tracks and the grooves 25 separating the second conductor tracks 26 from one another have a width which is determined substantially exclusively by the etching mask used. The first conductor tracks 24 and the second conductor tracks 26 form the word lines and bit lines of the memory matrix.

[0042] A lithography was used in the present example with an accuracy of 0.5 µm, while in addition phase-shifting techniques were used such as described, for example, in an article by M.D. Levenson in Microlithography World, Sep/Oct 1992, pp. 6-12, entitled "Phase-Shifting Mask Strategies: Line-Space Patterns". Such techniques are particularly suitable for comparatively simple structures such as that of the present memory matrix which comprises substantially only a number of continuous tracks. As a result, the widths of the various conductor tracks 24, 26 and grooves 25, 27 can be constructed to be smaller by approximately a factor two than the minimum lithographical dimension ℓ of 0.5 µm associated with the lithography used. In this example, accordingly, the said widths are equal to $\ell/2$ or 0.25 µm. Even smaller dimensions can be achieved with advanced optical lithography or with imaging techniques which use radiation of a shorter wavelength than visible light such as, for example, UV, X-ray and electron lithography.

[0043] As is shown in plan view in Fig. 2B, a memory cell including the associated insulation can be realised on a chip area of no more than ℓ^2, or 0.25 µm^2, in the present embodiment. The memory element proper 4, 5, 6 then occupies no more than $\ell^2/4$. This is an order of magnitude less than the area required for the known memory cell. As a result, the invention realises an information density of approximately 400 Mbit/cm^2 in the case of 0.5 µm lithography and is thereby extremely - though not exclusively - suitable for applications in which such a large non-volatile memory capacity is desired such as, in addition to many computer applications, for example, also in audio and/or video memories. Thus, for example, the memory contents of a conventional Compact Disc (CD) with an hour of digital stereo music information can be stored on less than 2 cm^2 in the device according to the present invention, using data compression techniques known *per se*. The invention has the additional advantage that the memory can be read fully electronically, so that no moving parts which require space and energy and are comparatively prone to failure are required. For ease of handling and for the possible display of information relating to the music and/or images stored, the device may be constructed, for example, as a chip card.

[0044] A third embodiment of the device according to the invention is shown in Fig. 3. This embodiment starting material is a comparatively lightly doped p-type silicon substrate 1 which is provided with a partly recessed silicon oxide pattern 31 at the surface 30 by means of local oxidation. The oxide pattern 31 encloses two islands 32, 42 which are doped somewhat more heavily than the substrate 1, n-type and p-type, respectively, by means of ion implantation.

[0045] A PMOS transistor is present at the surface 30 in the n-type island 32 with a comparatively heavily doped p-type source zone 33 and drain zone 34 which are mutually separated by a portion of the n-type island 32, which portion forms a channel region 35 of the transistor. The transistor further comprises a gate electrode 36 which is separated from the channel region 35 by a comparatively thin gate dielectric 37 of silicon oxide. The gate electrode 36 comprises n-type polycrystalline silicon and is coated with titanium silicide which is electrically comparatively well-conducting as compared with the polycrystalline silicon, and which thus reduces the electrical resistance of the gate electrode 36. The electrical conductance of the channel region 35 can be modulated by means of the gate electrode 36. The source zone 33 and drain zone 34 are provided with a source electrode 38 and a drain electrode 39, respectively, of titanium silicide as electrical connections.

[0046] The p-type island 42 in an analogous manner comprises an NMOS transistor with a comparatively heavily doped n-type source zone 43 and drain zone 44 which are mutually separated by a p-type channel region 45. The channel region 45 is covered in that order with a comparatively thin gate dielectric 47 of silicon oxide and a gate electrode 46 of n-type silicon by means of which the conductance in the channel region 45 can be controlled. To achieve a lower electrical resistance, the gate electrode 46 is provided with a comparatively well-conducting top layer of titanium silicide. The source and drain zones 43, 44 are provided with well-conducting source and drain electrodes 48, 49, respectively, of titanium silicide. The drain elec-

trodes 39, 49 of the two transistors are integral.

[0047] The source and drain electrodes 38, 48, 39, 49 and the top layers of the gate electrodes 36, 46 of the two transistors are provided in one and the same process step. Instead of titanium silicide, indeed, other silicides, for example, cobalt silicide and platinum silicide, may be used, or possibly a metal such as, for example, titanium-tungsten and aluminium, may be used.

[0048] The entire assembly is coated with an approximately 0.5-1 μm thick dielectric intermediate layer 50, in the present case of flow glass (BPSG) which has a substantially plane surface 51 in spite of the subjacent structure. Such a plane surface 51 may be obtained in that the assembly is heated to a temperature of approximately 900° C after the layer 50 was provided, whereby the layer 50 flows and smoothes itself out. In principle, alternative glass types including pure silicon oxide may also be used for this purpose. However, these have the disadvantage that the softening temperatures of these materials are substantially higher. Alternatively, an insulating layer may be applied which, thereafter is planarized in a known manner, for instance by applying photoresist and etch-back.

[0049] The dielectric intermediate layer 50 separates a matrix of memory cells from the subjacent substrate 1 with the transistors present therein. In this way the transistors forming part of the electronics by which the memory cells can be controlled during operation can be integrated below the memory matrix, so that no or hardly any additional space is required for the control. The control electronics are coupled to the memory matrix through openings in the intermediate layer 50.

[0050] The matrix is formed by a number (n) of mutually parallel first conductor tracks 54 which comprise a top layer of p-type silicon, and a number (m) of mutually parallel second conductor tracks 56 of n-type silicon. In Fig. 3 four tracks 54 and one track 56 are shown. The first conductor tracks 54 lie on the dielectric intermediate layer 50 which isolates the conductor tracks 54 from the subjacent substrate 1 and the transistors present therein. The second conductor tracks 56 cross the first conductor tracks 54 in a direction transverse thereto and are separate from the first conductor tracks 54 by an approximately 8 nm thick insulating layer 5 of, in that order, approximately 6 nm silicon nitride and approximately 2 nm silicon oxide. Wherever a first conductor track 54 and a second conductor track 56 overlap, there is a memory element comprising a semiconductor region 4 of p-type silicon forming part of the relevant first conductor track 54 and a conductor region 6 of n-type silicon formed by the relevant second conductor track 56. The memory cells, furthermore, are each provided with a contact region 3 of tungsten silicide which lies in the first conductor track 54 below the semiconductor region 4.

[0051] The memory matrix according to the invention is of a comparatively simple construction and may be provided in a comparatively late stage in the manufacturing process. In addition, the device is compatible with many kinds of semiconductor processes, *i.e.* besides in a CMOS process as in the present example, for example, also in uni-channel MOS processes and in bipolar processes.

[0052] In the present example, the memory matrix is not provided until after the transistors have been formed and the dielectric intermediate layer 50 has been provided. For this purpose, a conductive layer for the contact regions 3 and a p-type doped silicon layer, for example in polycrystalline form, are deposited in that order on the dielectric intermediate layer 50, after which the two layers are etched into a pattern so as to shape the first conductor tracks 54. The layers between the tracks 54 to be formed are removed down to the dielectric intermediate layer 50 during this. The grooves 55 thus formed extend down to the dielectric intermediate layer 50 and thus form an isolation region comparable to region 7 of Fig. 1 which isolation region bounds both the semiconductor regions 4 and the subjacent contact regions 3 at opposing sides, thus ensuring a good mutual isolation of the first conductor tracks 54.

[0053] After the first conductor tracks 54 have been provided, the assembly is covered in that order with a layer of silicon nitride and a layer of silicon oxide which serve as a dielectric 5 for the memory elements to be formed, and in addition coat the grooves 55 situated between the first conductor tracks 54. On the insulating layer is then provided an n-type silicon layer from which the second conductor tracks 56 are etched. In this embodiment, again, a 0.5 μm lithography is used at least for forming the memory matrix in conjunction with phase-shifting techniques, so that the memory elements 4, 5, 6 including the associated portions of the insulating region 7, 55 occupy no more than approximately 0.25 μm^2 chip area.

[0054] Although the invention was described above with reference to only a few embodiments, it will be obvious that the invention is by no means limited to the examples given. Many more variations are possible to those skilled in the art within the scope of the invention which is defined by the attached claims. Thus the conductivity types mentioned for the semiconductor materials used may be replaced, all simultaneously, by the opposite conductivity types.

[0055] The programmable element may be used not only in a memory cell, but also, for example, as a programmable logic switch. Furthermore, the rectifying junction formed after programming may form part of a kind of semiconductor switching element different from a diode. In particular, the rectifying junction may form, for example, the emitter-base junction of a bipolar transistor. The transistor may be formed selectively in this manner.

[0056] The device according to the invention may be provided on any suitable substrate. In particular, it is possible to start with a substrate comprising a semiconductor body with a (monocrystalline) top layer of semi-

conductor material which is separated from the rest of the semiconductor body by a dielectric intermediate layer. Such a structure is usually called SOI (Silicon On Insulator). In that case, the conductor region or the semiconductor region of the programmable element may be formed from the top layer, for example, and the isolating region preferably extends down to the dielectric intermediate layer.

[0057] In addition, it is possible to start with a fully dielectric substrate, for example, made of glass, in which case thin-film transistors may be used for the control function.

[0058] In general, the invention provides a semiconductor device in which a programmable element can be integrated with an extremely high packing density.

Claims

1. A semiconductor device with a programmable element comprising a doped semiconductor region (4) and a conductor region (6) which are separated from one another by at least a portion of an insulating layer (5), said insulating layer having a thickness such that, during programming, breakdown may occur in the insulating layer upon applying a voltage between the conductor region (6) and the semiconductor region (4), the conductor region (6) comprising a material which is suitable for forming a rectifying junction with the material of the semiconductor region (4), the programmable element further comprising a contact region (3) which forms an ohmic contact with the semiconductor region (4) and which has a comparatively low electrical resistivity compared therewith, characterized in that the contact region (3) is provided at a side of the semiconductor region (4) remote from the insulating layer (5) and is separated from the insulating layer (5) by the semiconductor region (4), and in that both the semiconductor region (4) and the contact region (3) are together laterally bounded by a dielectric isolation region (7) at mutually opposing sides.

2. A semiconductor device as claimed in Claim 1, characterized in that the isolation region comprises a groove which bounds the semiconductor region and the contact region laterally and which is coated with at least an insulating layer.

3. A semiconductor device as claimed in Claim 2, characterized in that the groove is filled up with a suitable filler.

4. A semiconductor device as claimed in any one of the Claims 1 to 3, characterized in that both the semiconductor region and the contact region form part of a first strip-shaped conductor track which is laterally bounded by the isolation region and in that the conductor region forms part of a second strip-shaped conductor track which extends transverse to the direction of the first conductor track.

5. A semiconductor device as claimed in Claim 4, characterized in that the first conductor track is formed by a first semiconductor track of a first conductivity type, and in that the contact region comprises a comparatively heavily doped buried semiconductor zone of the first conductivity type.

6. A semiconductor device as claimed in Claim 5, characterized in that the second conductor track comprises a second semiconductor track of a second, opposite conductivity type which is provided over the first semiconductor track.

7. A semiconductor device as claimed in Claim 5, characterized in that the second conductor track comprises a material which is suitable for forming a rectifying Schottky junction with the first conductor track.

8. A semiconductor device as claimed in Claim 5, 6 or 7, characterized in that the first semiconductor track is situated on a semiconductor substrate, in that the first conductor track forms a pn junction at least with a surface region of the semiconductor substrate, which pn junction is reverse biased during operation, and in that the isolating region which laterally bounds the first semiconductor track extends at least up to the surface region.

9. A semiconductor device as claimed in any one of the Claims 4 to 7, characterized in that the first conductor track is provided on a dielectric intermediate layer which separates the first conductor track from a subjacent semiconductor substrate, and in that the isolating region which laterally bounds the first conductor track extends down to the dielectric intermediate layer.

10. A semiconductor device as claimed in Claim 9, characterized in that the first conductor track is formed by a composite layer comprising a bottom layer containing metal which bottom layer adjoins the dielectric intermediate layer and of which the contact region forms part, and comprising a top layer of semiconductor material which top layer adjoins the insulating layer and of which the semiconductor region forms part.

11. A semiconductor device provided with a matrix of memory cells which each comprise a programmable element as claimed in any one of the preceding Claims, characterized in that the matrix is composed of a number (n) of parallel first conductor tracks which extend in a first direction and by a number (m) of parallel second conductor tracks

which extend in a second direction transverse to the first direction, in that the first conductor tracks are laterally bounded by strip-shaped isolating regions, and in that the first conductor tracks and the second conductor tracks are separated from one another by the insulating layer.

12. A semiconductor device as claimed in Claim 11, characterized in that the matrix is separated from a subjacent semiconductor body by a dielectric intermediate layer, and in that at least a semiconductor switching element is provided below the matrix in the semiconductor body.

13. A semiconductor device as claimed in Claim 12, characterized in that the dielectric intermediate layer is locally provided with an opening and in that a main electrode of the semiconductor switching element and a conductor track of the matrix are electrically interconnected through said opening.

Patentansprüche

1. Halbleiteranordnung mit einem programmierbaren Element, die ein dotiertes Halbleitergebiet (4) und ein Leitergebiet (6) umfasst, die voneinander durch zumindest einen Abschnitt einer Isolierschicht (5) getrennt sind, wobei die genannte Isolierschicht eine solche Dicke hat, dass während des Programmierens beim Anlegen einer Spannung zwischen dem Leitergebiet (6) und dem Halbleitergebiet (4) in der Isolierschicht Durchbruch auftreten kann, wobei das Leitergebiet (6) ein Material umfasst, das zum Bilden eines Gleichrichterübergangs mit dem Material des Halbleitergebietes (4) geeignet ist, wobei das programmierbare Element weiterhin ein Kontaktgebiet (3) umfasst, das mit dem Halbleitergebiet (4) einen ohmschen Kontakt bildet und das im Vergleich dazu einen verhältnismäßig geringen spezifischen elektrischen Widerstand hat, dadurch gekennzeichnet, dass das Kontaktgebiet (3) an einer von der Isolierschicht (5) abgewandten Seite des Halbleitergebiets (4) vorgesehen ist und von der Isolierschicht (5) durch das Halbleitergebiet (4) getrennt ist und dass sowohl das Halbleitergebiet (4) als auch das Kontaktgebiet (3) zusammen lateral durch ein Isolationsgebiet (7) an einander gegenüber liegenden Seiten begrenzt werden.

2. Halbleiteranordnung nach Anspruch 1, dadurch gekennzeichnet, dass das Isolationsgebiet einen Graben umfasst, der das Halbleitergebiet und das Kontaktgebiet lateral begrenzt und der mit zumindest einer Isolierschicht überzogen ist.

3. Halbleiteranordnung nach Anspruch 2, dadurch gekennzeichnet, dass der Graben mit einem geeigneten Füllmaterial aufgefüllt ist.

4. Halbleiteranordnung nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, dass sowohl das Halbleitergebiet als auch das Kontaktgebiet Teil einer ersten streifenförmigen Leiterbahn sind, die durch das Isolationsgebiet lateral begrenzt wird und dass das Leitergebiet Teil einer zweiten streifenförmigen Leiterbahn ist, die quer zur Richtung der ersten Leiterbahn verläuft.

5. Halbleiteranordnung nach Anspruch 4, dadurch gekennzeichnet, dass die erste Leiterbahn von einer ersten Halbleiterbahn eines ersten Leitungstyps gebildet wird, und dass das Kontaktgebiet eine verhältnismäßig stark dotierte vergrabene Halbleiterzone des ersten Leitungstyps umfasst.

6. Halbleiteranordnung nach Anspruch 5, dadurch gekennzeichnet, dass die zweite Leiterbahn eine zweite Halbleiterbahn eines zweiten, entgegengesetzten Leitungstyps umfasst, die über der ersten Halbleiterbahn vorgesehen ist.

7. Halbleiteranordnung nach Anspruch 5, dadurch gekennzeichnet, dass die zweite Leiterbahn ein Material umfasst, das geeignet ist, mit der ersten Leiterbahn einen gleichrichtenden Schottky-Übergang zu bilden.

8. Halbleiteranordnung nach Anspruch 5, 6 oder 7, dadurch gekennzeichnet, dass die erste Halbleiterbahn auf einem Halbleitersubstrat liegt, dass die erste Leiterbahn zumindest mit einem Oberflächengebiet des Halbleitersubstrats einen pn-Übergang bildet, wobei der pn-Übergang im Betrieb in Sperrrichtung vorgespannt ist, und dass das Isolationsgebiet, das die erste Halbleiterbahn lateral begrenzt, sich zumindest bis zum Oberflächengebiet hinauf erstreckt.

9. Halbleiteranordnung nach einem der Ansprüche 4 bis 7, dadurch gekennzeichnet, dass die erste Leiterbahn auf einer dielektrischen Zwischenschicht vorgesehen ist, die die erste Leiterbahn von einem darunter liegenden Halbleitersubstrat trennt, und dass das Isolationsgebiet, das die erste Leiterbahn lateral begrenzt, sich bis zur dielektrischen Zwischenschicht hinab erstreckt.

10. Halbleiteranordnung nach Anspruch 9, dadurch gekennzeichnet, dass die erste Leiterbahn von einer zusammengesetzten Schicht gebildet wird, die eine Metall enthaltende untere Schicht umfasst, die an die dielektrische Zwischenschicht grenzt und von der das Kontaktgebiet ein Teil ist, und die eine obere Schicht aus Halbleitermaterial umfasst, die an die Isolierschicht grenzt und von der das Halbleitergebiet ein Teil ist.

11. Halbleiteranordnung mit einer Matrix aus Speicherzellen, die jeweils ein programmierbares Element nach einem der vorhergehenden Ansprüche umfassen, dadurch gekennzeichnet, dass die Matrix aus einer Anzahl (n) paralleler erster Leiterahnen zusammengesetzt ist, die sich in einer ersten Richtung erstrecken, und einer Anzahl (m) paralleler zweiter Leiterbahnen, die sich in einer zweiten Richtung quer zur ersten Richtung erstrecken, dass die ersten Leiterbahnen durch streifenförmige Isolationsgebiete lateral begrenzt werden und dass die ersten Leiterbahnen und die zweiten Leiterbahnen voneinander durch die Isolierschicht getrennt sind.

12. Halbleiteranordnung nach Anspruch 11, dadurch gekennzeichnet, dass die Matrix durch eine dielektrische Zwischenschicht von einem darunter liegenden Halbleiterkörper getrennt ist und dass unter der Matrix in dem Halbleiterkörper zumindest ein Halbleiterschaltelement vorgesehen ist.

13. Halbleiteranordnung nach Anspruch 12, dadurch gekennzeichnet, dass die dielektrische Zwischenschicht örtlich mit einer Öffnung versehen ist und dass eine Hauptelektrode des Halbleiterschaltelementes und eine Leiterbahn der Matrix durch die genannte Öffnung hindurch elektrisch miteinander verbunden sind.

Revendications

1. Dispositif semi-conducteur muni d'un élément programmable comprenant une région semi-conductrice dopée (4) et une région conductrice (6), qui sont séparées, l'une de l'autre, par au moins une partie d'une couche isolante (5), ladite couche isolante présentant une épaisseur telle que, lors de la programmation, il peut se produire un claquage dans la couche isolante dans le cas d'application d'une tension entre la région conductrice (6) et la région semi-conductrice (4), la région conductrice (6) contenant un matériau qui est approprié à la formation d'une jonction redresseuse avec le matériau de la région semi-conductrice (4), l'élément programmable comprenant en outre une région de contact (3), qui forme un contact ohmique avec la région semi-conductrice (4) et qui présente une résistivité électrique relativement basse comparativement à cette dernière, caractérisé en ce que la région de contact (3) est appliquée d'un côté de la région semi-conductrice (4) éloigné de la couche isolante (5) et est séparée de la couche isolante (5) par la région semi-conductrice (4) et en ce que tant la région semi-conductrice (4) que la région de contact (3) sont ensemble latéralement délimitées par une région d'isolement diélectrique (7) des côtés mutuellement opposés.

2. Dispositif semi-conducteur selon la revendication 1, caractérisé en ce que la région d'isolement comprend une rainure qui délimite la région semi-conductrice et la région de contact latéralement et qui est revêtue d'au moins une couche isolante.

3. Dispositif semi-conducteur selon la revendication 2, caractérisé en ce que la rainure est remplie d'une substance de remplissage appropriée.

4. Dispositif semi-conducteur selon l'une des revendications précédentes 1 à 3, caractérisé en ce que tant la région semi-conductrice que la région de contact font partie d'une première piste conductrice en forme de bande qui est latéralement délimitée par la région d'isolement et en ce que la région conductrice fait partie d'une deuxième piste en forme de bande qui s'étend transversalement par rapport à la direction de la première piste conductrice.

5. Dispositif semi-conducteur selon la revendication 4, caractérisé en ce que la première piste conductrice est formée par une première piste semi-conductrice d'un premier type de conductivité et en ce que la région de contact comprend une zone semi-conductrice enterrée relativement fortement dopée du premier type de conductivité.

6. Dispositif semi-conducteur selon la revendication 5, caractérisé en ce que la deuxième piste conductrice comprend une deuxième piste conductrice d'un deuxième type de conductivité opposé qui est appliquée sur la première piste semi-conductrice.

7. Dispositif semi-conducteur selon la revendication 5, caractérisé en ce que la deuxième piste conductrice contient un matériau qui est approprié à la formation d'une jonction Schottky redresseuse avec la première piste conductrice.

8. Dispositif semi-conducteur selon la revendication 5, 6 ou 7, caractérisé en ce que la première piste semi-conductrice est située sur un substrat semi-conducteur, en ce que la première piste conductrice forme une jonction pn au moins avec une région de surface du substrat semi-conducteur, laquelle jonction pn est polarisée transversalement pendant le fonctionnement, et en ce que la région isolante qui délimite latéralement la première piste semi-conductrice s'étend au moins jusqu'à la région de surface.

9. Dispositif semi-conducteur selon l'une des revendications précédentes 4 à 7, caractérisé en ce que la première piste conductrice est appliquée sur une couche semi-conductrice intermédiaire diélectrique qui sépare la première piste conductrice du substrat semi-conducteur sous-jacent et en ce que la

région isolante qui délimite latéralement la première piste conductrice s'étend jusqu'à la couche intermédiaire diélectrique.

10. Dispositif semi-conducteur selon la revendication 9, caractérisé en ce que la première piste conductrice est formée par une couche composée comprenant une couche inférieure contenant un métal, couche inférieure qui avoisine la couche intermédiaire diélectrique et dont fait partie la région de contact, et comprenant une couche supérieure réalisée en un matériau semi-conducteur, couche supérieure qui avoisine la couche isolante et dont fait partie la région semi-conductrice.

11. Dispositif semi-conducteur muni d'une matrice de cellules de mémoire qui comprennent chacune un élément programmable comme revendiqué dans l'une des revendications précédentes, caractérisé en ce que la matrice est composée d'un nombre déterminé (n) de premières pistes conductrices parallèles, qui s'étendent dans une première direction et par un nombre déterminé (m) de deuxièmes pistes conductrices parallèles qui s'étendent dans une deuxième direction transversale par rapport à la première direction, en ce que les premières pistes conductrices sont délimitées latéralement par des régions isolantes en forme de bande, et en ce que les premières pistes conductrices et les deuxièmes pistes conductrices sont séparées, les unes des autres, par la couche isolante.

12. Dispositif semi-conducteur selon la revendication 11, caractérisé en ce que la matrice est séparée d'un corps semi-conducteur sous-jacent par une couche intermédiaire diélectrique et en ce qu'au moins un élément de commutation semi-conducteur est appliqué au-dessous de la matrice dans le corps semi-conducteur.

13. Dispositif semi-conducteur selon la revendication 12, caractérisé en ce que la couche intermédiaire diélectrique est munie localement d'une ouverture et en ce qu'une électrode principale de l'élément de commutation semi-conducteur et une piste conductrice de la matrice sont interconnectés électriquement à travers ladite ouverture.

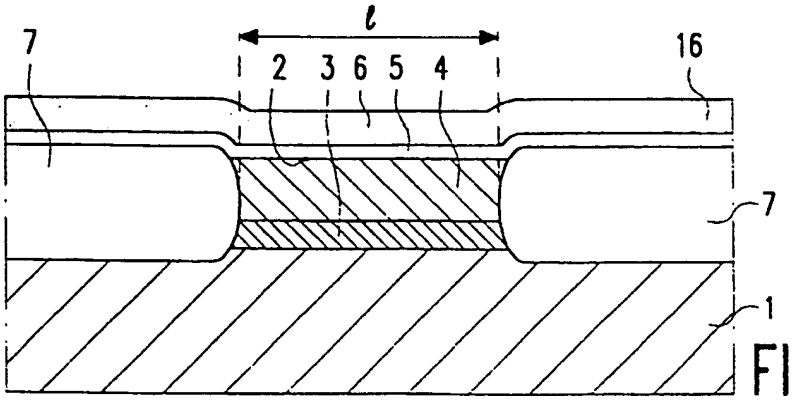

FIG. 1a

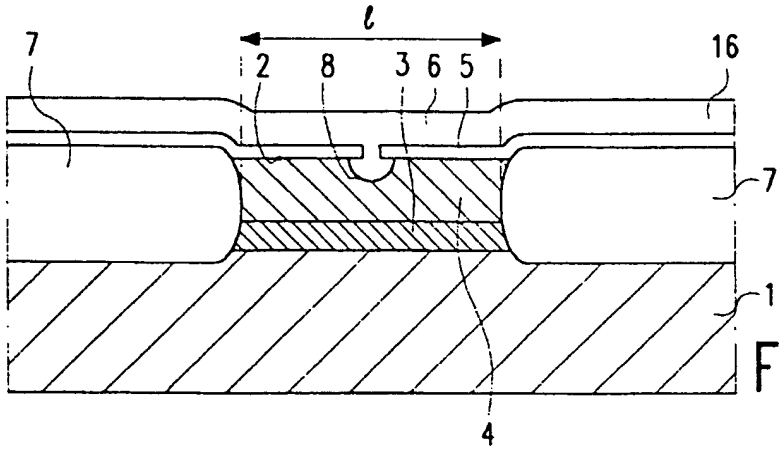

FIG. 1b

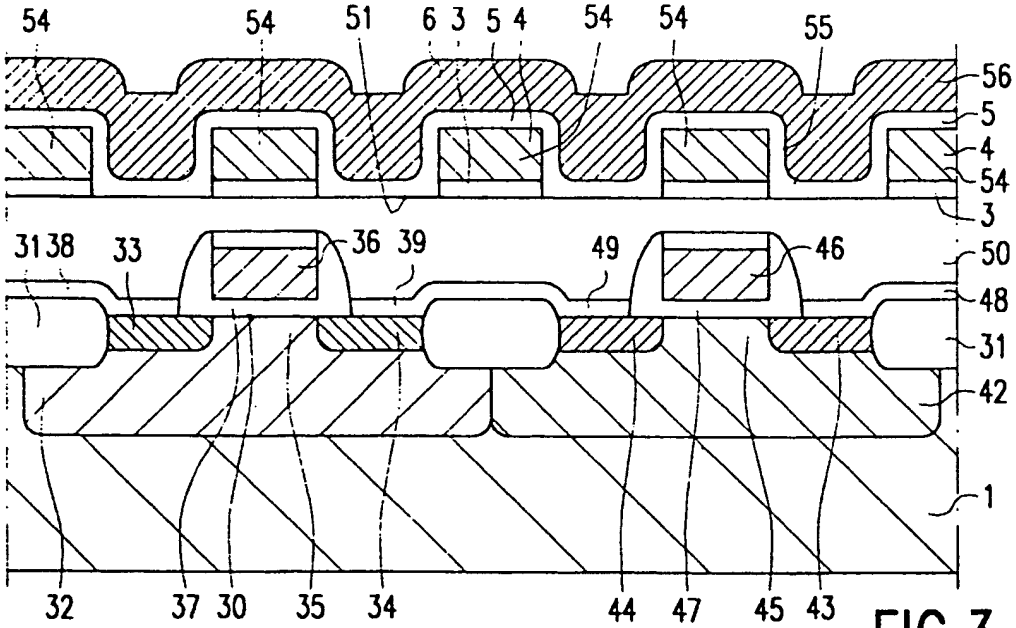

FIG.3

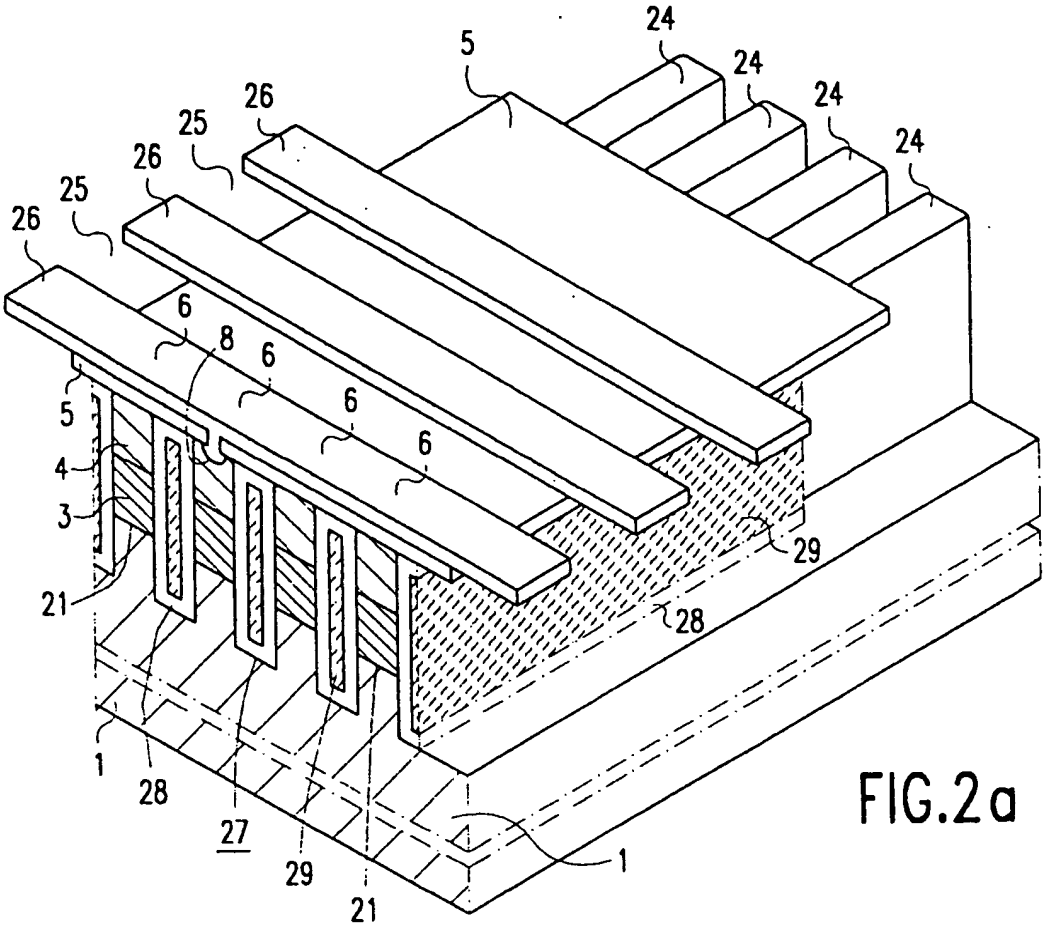
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FIG.2a

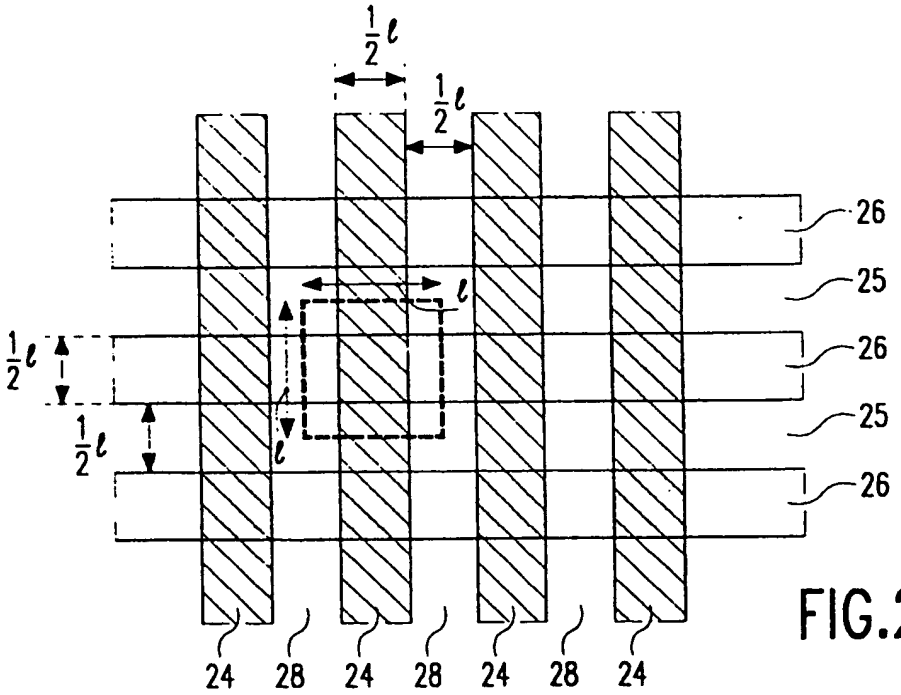
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FIG.2b